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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,034	08/04/2003	Chih-Yuh Yang	H1174	4699

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EXAMINER	
ABRAHAM, FETSUM	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,034	YANG ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-14* is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The election made on 5/11/04 has been acknowledged and the non elected claims 10-14 withdrawn from consideration.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-4 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: said first and second gates in relation to the single gate in claim surrounding said fin. The gate structure in the independent claim 1 is a single gate and is claimed to surround all surfaces of said fin. In light of this physical realization, it is not clear how the two gates in claim 2 fit into the structural configuration of the structure in claim 1.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,5,6,9 are rejected under 35 U.S.C. 102(a) as being anticipated by Judy Xilin et al.

The article "GERMANIUM MOSFET DEVICES AND METHODS FOR MAKING THE SAME" discloses a FINFET in figure 24 composed of a substrate,

an insulation layer on the substrate, an SOI layer on the insulation layer and a fin (2010) having side, top and bottom surfaces formed on the insulation layer and all side surfaces fully or partially surrounded by gate layer (2410) at the channel region of the overall structure.

As for claim 5, the gate insulation layer partially or fully surrounds all sides or surfaces of the fin.

As for claim 6, there is a gate dielectric layer on the top surface of the fin.

As for claim 9, the prior art possesses the claimed source/drain and buried insulation specifications because it is an SOI based TFT.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7,8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Judy Xilin et al.

Although the prior art omits to teach a multi-layered gate insulation structure around the fin, a composite gate insulation layer of oxide and nitride is notoriously utilized in the art because the arrangement allows to modulate gate insulation thickness and dielectric constant by best utilizing the dielectric constant differences of the materials.

As for claim 8, gate insulation layer thickness is one of the most common variables in the art of MOSFETs that differ from a design to another based on

anticipated gate capacitance, insulation breakdown voltages, and threshold voltages for the claimed multi layered gate insulation to be obvious for usage in any other MOSFET based structures.

Claims 1,5,6,9 are rejected under 35 U.S.C. 102(a) as being anticipated by Yu et al (6,764,884).

The patent discloses a FINFET in figure 11D composed of a substrate, an insulation layer on the substrate, an SOI layer on the insulation layer and a fin (1120) having side, top and bottom surfaces formed on the insulation layer and all side surfaces surrounded by gate layer (1150) at the channel region of the overall structure.

As for claim 5, the gate insulation layer (1140) surrounds all sides or surfaces of the fin (1120).

As for claim 6, there is a dielectric layer (1140) on the top surface of the fin (1120).

As for claim 9, the prior art possesses the claimed source/drain and buried insulation specifications because it is an SOI based TFT.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7,8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the same art (PN: 6,764,884).

Although the prior art omits to teach a multi-layered gate insulation structure around the fin, a composite gate insulation layer of oxide and nitride is notoriously utilized in the art because the arrangement allows to modulate gate insulation thickness and dielectric constant by best utilizing the dielectric constant differences of the materials.

As for claim 8, gate insulation layer thickness is one of the most common variables in the art of MOSFETs that differ from a design to another based on anticipated gate capacitance, insulation breakdown voltages, and threshold voltages for the claimed multi layered gate insulation to be obvious for usage in any other MOSFET based structures.

Claims 15-20 have been allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
1/20/04